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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/986,650	11/09/2001	Derek Ward	P67300US0	5599
136 7590 12/16/2008 JACOBSON HOLMAN PLLC 400 SEVENTH STREET N.W. SUITE 600 WASHINGTON, DC 20004				
EXAMINER JARRETT, RYAN A				
ART UNIT 2121		PAPER NUMBER		
MAIL DATE 12/16/2008		DELIVERY MODE PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

09/986,650

Applicant(s)

WARD, DEREK

Examiner

RYAN A. JARRETT

Art Unit

2121

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 September 2008.
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 3, 4, 8-19, 22-26, 29-31 and 33-42 is/are pending in the application.
4a) Of the above claim(s) 8-19, 23-26 and 29-31 is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 3, 4, 22 and 33-42 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on 09 November 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 09/12/08 has been entered.

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Response to Arguments

Applicant's arguments, see pages 19-22, filed 09/12/08, with respect to the specification objections and rejections under 35 U.S.C. 112 1st paragraph have been fully considered and are persuasive. The previous specification objections and rejections under 35 U.S.C. 112 1st paragraph have been withdrawn.

Applicant's arguments, see pages 22-23, filed 09/12/08, with respect to the rejections under 35 U.S.C. 112 2nd paragraph have been fully considered and are persuasive. The previous rejections under 35 U.S.C. 2nd paragraph have been withdrawn.

Applicant's arguments, see pages 23-29, filed 09/12/08, with respect to the rejection(s) of claim(s) 3, 4, and 22 under 35 U.S.C. 102(b) as being anticipated by "Virtex-E" have been fully considered and are mostly persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of How et al. US 6,611,932.

Applicant's arguments, see pages 29-32, filed 09/12/08, with respect to previous claims 27 and 28 (current claims 40 and 41) have been fully considered and are persuasive. The 35 U.S.C. 103(a) rejections based on New et al. US 6,091,263 have been withdrawn.

Claim Objections

Claims 3, 4, and 34-37 are objected to because of the following informalities:

Claim 3 recites the limitation "logic circuit" in line 8. It appears that this should be changed to "logic processing circuit" since it is subsequently referred to as such in the claim(s).

Claim 3 recites the limitation "said input interfaces and said output interfaces" in line 11. There is insufficient antecedent basis for this limitation in the claim since this was previously referred to as "at least one digital input interface" and "at least one digital output interface" in lines 3-4.

Claim 4 (and 35) recites the limitation "said first plurality of logic processing flip-flops" in lines 14-15. There is insufficient antecedent basis for this limitation in the claim since this was previously referred to as "said plurality of logic processing flip-flops". There doesn't appear to be any separate *first* or *second* sets of flip-flops.

Claim 22 (and 36) recites the limitation "the levels of the output signals" in line 4. There is insufficient antecedent basis for this limitation in the claim. There does not appear to be any prior mention of levels or output signals.

Claim 34 (and 37) recites the limitation "said output registers" in line 7. There is insufficient antecedent basis for this limitation in the claim since this was previously referred to as "at least one output register".

Claim 34 (and 37) recites the limitation "the output signal(s)" and "the level last sampled" in lines 8-9. There is insufficient antecedent basis for this limitation in the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 4, 22, and 33-42 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Regarding claims 4 and 35, Examiner cannot find support in the specification for a “first mode” that operates in the first condition but not in the second condition, and a “second mode” that operates in both the first and second condition. Examiner understands that there is support for a first condition (shift register condition) and a second condition (normal logic processing condition), but does not see any support for the claimed “first and second modes” in addition to the conditions.

Regarding claim 33, Examiner cannot find support in the specification for the features of this claim. Applicant states that support for this claim can be found in the 'relocation of state data section' of the specification, but there is no mention of any flip-flop "ordering" in this section of the specification.

Claims 22, 34-42 depend from claims 4, 33, and 35 and thus incorporate the same deficiencies.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 3, 4, 22, 33, 35, and 36 are rejected under 35 U.S.C. 102(e) as being anticipated by How et al. US 6,611,932. For example, How et al. discloses:

3. A programmable controller for use with a monitoring device, said programmable controller including:

at least one digital input interface,

at least one digital output interface for receiving data from at least one output register,

programmable logic hardware including a plurality of logic elements including flip-flops, and electrically configurable interconnections, said interconnections configurable to interconnect the logic elements as a logic circuit, said logic processing circuit arranged to implement a user control program defined by a user as a user control program circuit, said logic processing circuit configurable in said programmable logic hardware, and connected to said input interfaces and said output interfaces (e.g., abstract),

program loading circuits for configuring said programmable logic hardware with said logic processing circuit prior to initiating control, and where said programmable logic hardware, configured with the logic processing circuit (e.g., abstract), includes:

a plurality of logic processing circuit flip-flops for storing state data, and for each of these flip-flops, an associated support circuit, the support circuits arranged to operate selectively between first and second conditions (e.g., abstract: "each logic block is further equipped for addressable mode control"), wherein in said first condition (e.g., abstract: "freeze mode") the support circuits connect the flip-flops as a shift register for transporting state data into and out of the logic processing circuit (e.g., abstract: "When the logic blocks are selected to be frozen, the logic blocks behave as a series of daisy-chained master-slave flip-flops"), and wherein in the second condition (e.g., abstract: "normal mode") the support circuits connect the flip-flops as logic elements of said user control program (e.g., abstract: "normal mode is defined by the user-designed circuit"), the support circuits being selected to operate in only one of either the first condition or the second condition at any one time (e.g., abstract: "each logic block is further equipped for addressable mode control").

33. The programmable controller as claimed in claim 3 wherein the flip-flops connected as a shift register (e.g., abstract: "the logic blocks behave as a series of daisy-chained master-slave flip-flops") have their order in the shift register determined by programmable logic device configuration (e.g., abstract: "the user-designed circuit").

Allowable Subject Matter

Claims 34 and 37-42 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 1st and 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to teach or fairly suggest the features of claims 34 and 37, in combination with the remaining features and elements of the claimed invention.

Claims 40-42 depend from claim 34, and are thus allowable by virtue of this dependency.

Claims 38-39 depend from claim 37, and are thus allowable by virtue of this dependency.

Election/Restrictions

Claims 8-19, 23-26, 29, and 30 were previously withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 06/05/07.

Claim 31 was also previously withdrawn from consideration as being directed to a non-elected invention, based on original presentation. See 37 CFR 1.142(b) and MPEP § 821.03.

Claims 34 and 37 are allowable. The restriction requirement among inventions, as set forth in the Office action mailed on 04/12/07, has been reconsidered in view of the allowability of claims to the elected invention pursuant to MPEP § 821.04(a). **The restriction requirement is hereby withdrawn as to any claim that requires all the limitations of an allowable claim.** Claims 8-19, 23-26, and 29-31, remain withdrawn from further consideration because they do not require all the limitations of an allowable generic linking claim as required by 37 CFR 1.141.

In view of the above noted withdrawal of the restriction requirement, applicant is advised that if any claim presented in a continuation or divisional application is anticipated by, or includes all the limitations of, a claim that is allowable in the present application, such claim may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application. Once a restriction requirement is withdrawn, the provisions of 35 U.S.C. 121 are no longer applicable. See *In re Ziegler*, 443 F.2d 1211, 1215, 170 USPQ 129, 131-32 (CCPA 1971). See also MPEP § 804.01.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

How et al. US 6,223,313 discloses a method and apparatus for controlling and observing data a logic-based ASIC.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan A. Jarrett whose telephone number is (571) 272-3742. The examiner can normally be reached on 10:00-6:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ryan A. Jarrett/
Primary Examiner, Art Unit 2121

12/12/08